## REMARKS

Claims 1-21 are pending in this application after this Amendment. Claims 1, 4, 5, and 10-12 are independent. In light of the amendments and remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by *Mitchell et al.* (USP 5,987,614). Applicants respectfully traverse this rejection.

### Prior Art Rejections

In support of the Examiner's rejection of claim 1, the Examiner asserts that *Mitchell et al.* discloses a distributed power management system and method comprising a host 40 and a plurality of subsystems 51a-51n wherein each subsystem monitors a state of coupling with the host device, citing to col. 6, lines 7-21. Applicants respectfully disagree with the Examiner's characterization of this reference.

The disclosure of *Mitchell et al.* is directed to a distributed power management system and method for a computer. The structure and method seeks to reduce power consumption in a computer system without sacrificing computer performance or inhibiting a computer user's rapid access to the computer. Communications over a communications link such as a parallel bus, serial bus, or wireless

link, are monitored by each device to determine device identifiers communicated over the link and these identifiers are compared to the identifier associated with the monitoring device. Each device monitors the communications and is responsible for self-controlling its operating condition to minimize power consumption. Each device includes a first component which operates continuously to provide the monitoring function and a second component that operates in a low power consumption mode unless the first component signals the second component that its operation is needed during that time period. (Abstract).

Specifically, *Mitchell et al.* provides for a processor 40 placing the subsystem device addresses and bus clock signals on a central bus 80. Each subsystem 51a-51n includes an address monitor/decoder unit 91a-91n which is connected to receive device (subsystem) addresses communicated over the bus 80 and decode them. When a received and decoded address identifies a device associated with or controlled by the particular addressed subsystem, the subsystem bus interface 54a generates a subsystem select signal which it communicates to clock control logic 53a within the subsystem along the bus clock signal. (Col. 6, lines 7-17).

Additionally, as depicted in Fig. 3, the bus interface logic 54a-54n of each subsystem module runs off the bus clock signal 74 which is generated by central bus interface block 43 and routinely derived from the CPU processor clock signal, albeit at a slower

rate than the CPU clock, and each of the bus interface logic units 54n, continuously monitors activity, such as the occurrence of an address identified to that particular subsystem on an address bus 72. (Col. 7, lines 38-47). Upon detection of an address identified to that particular subsystem, core logic 1 responds to the gated clock signal and commences operation and exits from its power consumption saving state or mode. After the bus cycle is finished, and access to that particular subsystem has completed for that particular bus cycle, the subsystem deasserts the select signal so that gated bus clock 57 is stopped and the core logic component 52 of the subsystem then reenters its power saving mode. Power savings is achieved at the bus cycle level and no formal status or mode transitions, such as might be controlled by a state machine, are involved or required. (Col. 8, lines 1-11).

In contrast, the present invention as provided in claim 1 recites, *inter alia*, an image display system comprising at least one display device connected to a host device wherein an image is displayed on the at least one display device in accordance with an image signal which is output from the host device and the at least one display device monitors a state of coupling with the host device. While *Mitchell et al.* teaches a subsystem monitoring the occurrence of an address on an address bus, there is no teaching or suggestion in *Mitchell et al.* that is directed to the at least one display device monitoring a state of coupling with the host device.

As such, *Mitchell et al.* fails to anticipate the present invention. It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 2-3, 13, and 19-21 are allowable for the reasons set forth above with regard to claim 1 at least based upon their dependency on claim 1.

It is respectfully submitted that claim 4 contains elements similar to those discussed above with regard to claim 1 and, thus, claim 4, together with claims dependent thereon, are allowable for the reasons set forth above with regard to claim 1.

Further, it is respectfully submitted that there is no teaching or suggestion in *Mitchell et al.* that is directed to a display device determining a state of coupling based on a data enable signal which is output from the host device. As such, it is respectfully requested that the outstanding rejection be withdrawn.

With regard to claim 5, it is respectfully submitted that claim 5 contains elements similar to those discussed above with regard to claim 1 and, thus, claim 5, together with claims dependent thereon, are not anticipated by *Mitchell et al.*

Further, it is respectfully submitted that there is no teaching or suggestion in *Mitchell et al.* that is directed to determining a state of coupling with the host device based on a data transfer clock signal which is output from the host device. As *Mitchell et al.* fails to teach or suggest all of the claimed

elements, it is respectfully submitted that claim 5 is not anticipated by *Mitchell et al.* It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 10-12 contain elements similar to those discussed above with regard to claim 1 and thus these claims, together with claims dependent thereon, are allowable for the reasons set forth above with regard to claim 1.

**Conclusion**

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Charles Gorenstein, #29,271

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

CG/CMV/jdm
0717-0469P

(Rev. 02/12/2004)